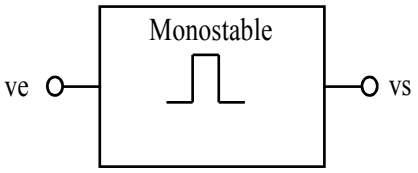
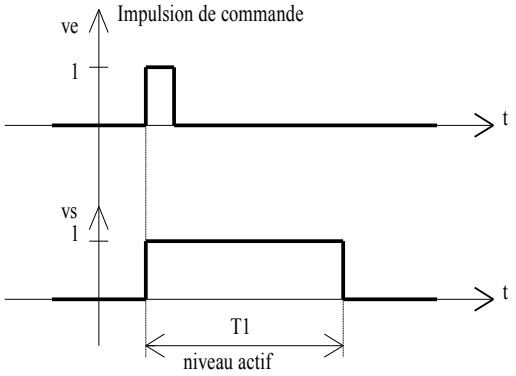
La fonction monostable

I. Définition

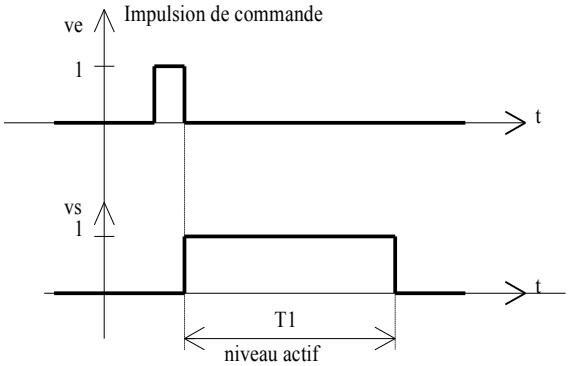
La fonction monostable génère une impulsion d'une durée déterminée. Cette impulsion est déclenchée par un signal de commande qui est, en règle générale, une impulsion de durée beaucoup plus courte que l'impulsion générée par la fonction.



II. Monostable à déclenchement sur front montant



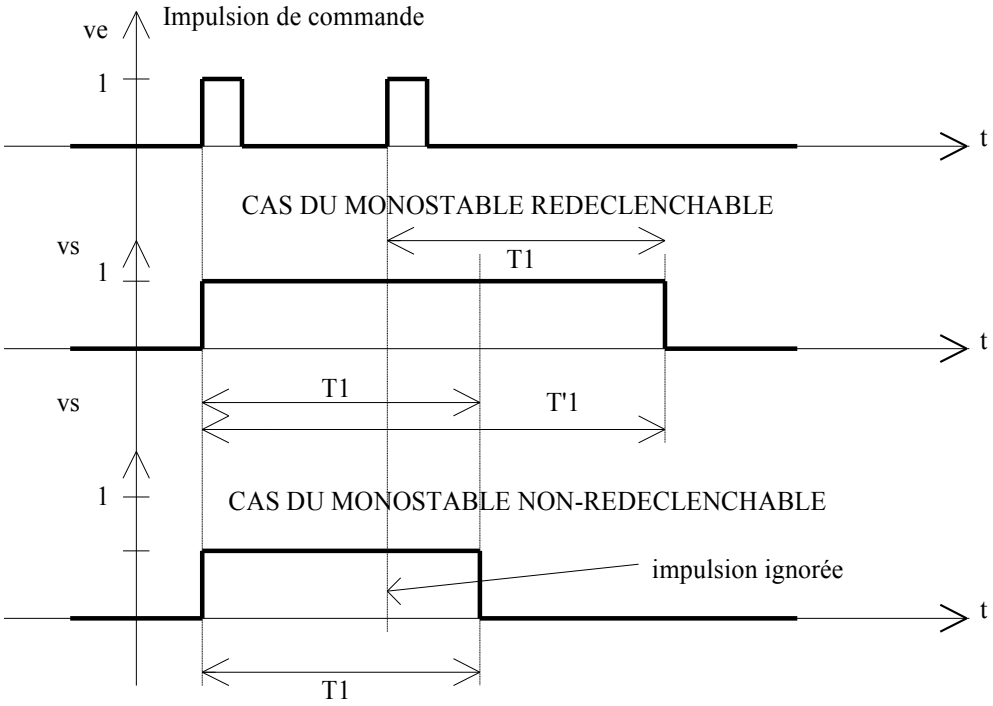
III. Monostable à déclenchement sur front descendant



IV. Monostable redéclenchable et non redéclenchable

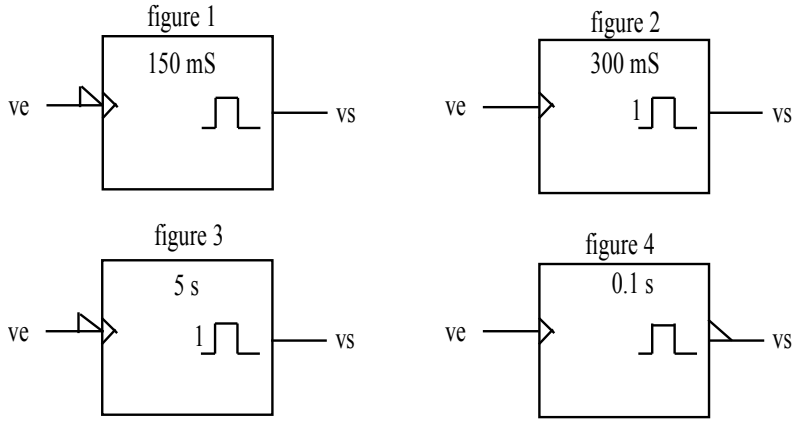
- **redéclenchable**: un monostable est dit redéclenchable si une impulsion de commande est prise en compte pendant le niveau actif (instable) de la sortie; dans ce cas, la durée du niveau actif est prolongée du temps T1.

- **non-redéclenchable**: un monostable est dit non-redéclenchable si une impulsion de commande n'est pas prise en compte pendant le niveau actif (instable) de la sortie; dans ce cas, la durée du niveau actif dure le temps T1 à partir du front actif de l'impulsion de commande précédente.



V. Représentation AFNOR

- figure 1: monostable redéclenchable actif sur front descendant
- figure 2: monostable non-redéclenchable actif sur front montant
- figure 3: monostable non-redéclenchable actif sur front descendant
- figure 4: monostable redéclenchable actif sur front montant avec sortie complémentée



VI. Exercice: utilisation du 74LS123 (voir documentation constructeur en annexe**)**

- réaliser la fonction monostable redéclenchable actif sur le front montant de ve et dont la durée de l'impulsion dure 100 ms.
- réaliser la fonction monostable non-redéclenchable actif sur le front descendant de ve et dont la durée de l'impulsion dure 200 ms.

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74LS123
Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-LOW transition trigger input and pin (B) is an active-HIGH transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (⌐‾). To obtain the best trouble free operation from this device please read the operating rules as well as the Fairchild Semiconductor one-shot application notes carefully and observe recommendations.

Features

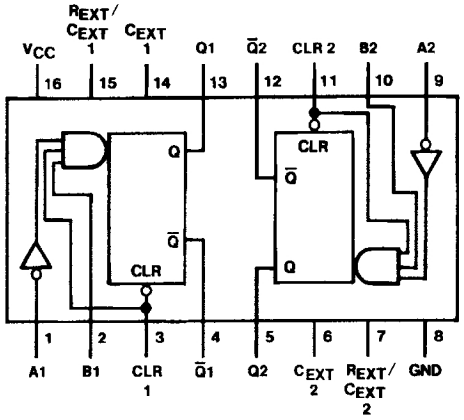
- DC triggered from active-HIGH transition or active-LOW transition inputs
- Retriggerable to 100% duty cycle
- Compensated for V_{CC} and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Ordering Code:

Order Number	Package Number	Package Description
DM74LS123M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS123SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS123N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌐‾	⌐‾
H	↓	H	⌐‾	⌐‾
↑	L	H	⌐‾	⌐‾

H = HIGH Logic Level
L = LOW Logic Level
X = Can Be Either LOW or HIGH
↑ = Positive Going Transition
↓ = Negative Going Transition
⌐‾ = A Positive Pulse
⌐‾ = A Negative Pulse

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-LOW transition or active-HIGH transition inputs or be reduced by use of the active-LOW or CLEAR input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the DM74LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation. Furthermore, if a polarized timing capacitor is used on the DM74LS123 the negative terminal of the capacitor should be connected to the "C_{EXT}" pin of the device (Figure 1).

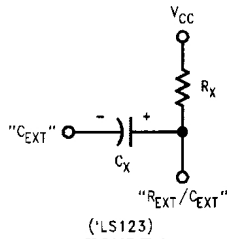


FIGURE 1.

3. For $C_X >> 1000$ pF the output pulse width (t_W) is defined as follows:

   $t_W = KR_X C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [t_W is in ns]

   K = 0.37
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

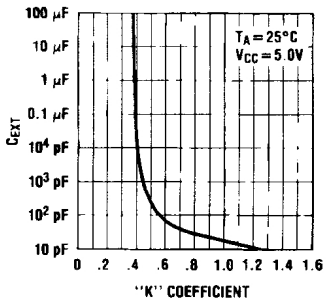


FIGURE 2.

5. For $C_X < 1000$ pF see Figure 3 for t_W vs. C_X family curves with R_X as a parameter:

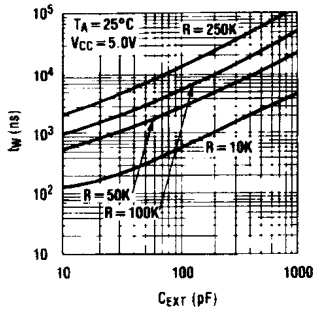


FIGURE 3.

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

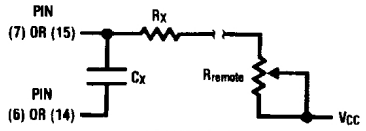


FIGURE 4.

"R_{remote}" should be as close to the device pin as possible.

7. The retriggerable pulse width is calculated as shown below:

   $T = t_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$

   The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 5).

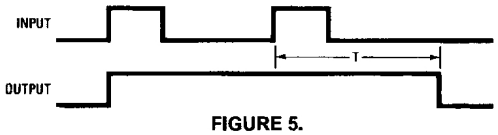


FIGURE 5.