TD LES MEMOIRES

A/

I/ Une mémoire a un bus des adresses de 20 fils et un bus des données de 8 fils. Calculer le nombre de cases mémoire disponibles dans ce composant. Calculer la valeur minimum et maximum (en hexadécimal) que peut avoir cette case mémoire

II/ Quelle est la différence entre une mémoire morte ROM et une mémoire vive RAM.

B/ Etude du schéma structurel (Voir annexe 1)

1) Quelle est la taille du bus des adresses en décimal, en hexadécimal, en bits (rappel: 1K en informatique vaut 1024 bits)

2) Quelle sont les valeurs maximum et minimum des adresses du bus des adresses.

3) Donner la taille du bus des données, la valeur maximum et minimum des données présentes sur le bus.

4) Déterminer le type de mémoire que sont U_1 et U_2. Donner leurs caractéristiques: taille des bus, nombre de cases mémoires disponibles.

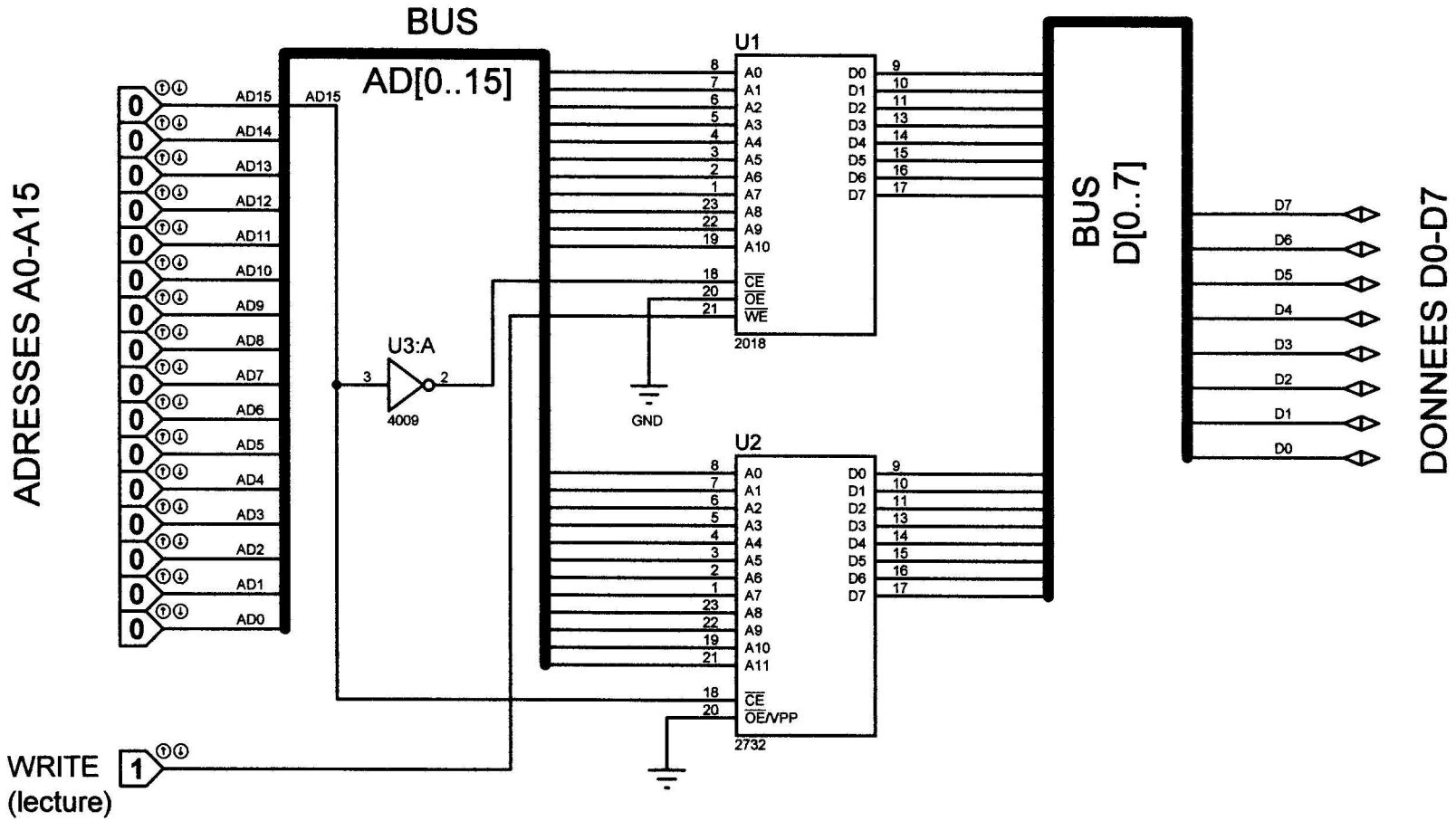
5) Déterminer les valeurs de A_{12} à A_{15} pour que U_1 soit sélectionnée (binaire et hexadécimal)

6) Déterminer les valeurs de A_0 à A_{15} pour que U_2 soit sélectionné (binaire et hexadécimal)

7) Compléter le document en annexe 2.

Annexe 1

LES MEMOIRES



6. CONTENU PARTIEL DE L'EPROM

6.1. LA MELODIE :

L'EPROM contient des informations de la mélodie.

Adr(@)	@+0	@+1	@+2	@+3	@+4	@+5	@+6	@+7	@+8	@+9	@+A	@+B	@+C	@+D	@+E	@+F
$8000	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80
$8010	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80	$80
$8020	$C0	$CC	$BA	$9F	$73	$5B	$63	$92	$B4	$9D	$8F	$90	$97	$9F	$97	$85
$8030	$49	$25	$2B	$4B	$69	$72	$73	$73	$6B	$82	$A2	$8A	$5B	$38	$40	$5A

Tableau 1 : Contenu partiel de la mémoire EPROM **MELODIE**

6.2. LA FREQUENCE DE TEST :

L'EPROM contient également des informations qui permettent de mettre au point la carte de câblage imprimé. Le contenu de la mémoire en mode sinus est donné par le *tableau 2*. La capacité de l'EPROM est de 32 Koctets. La durée d'un octet est également de 81,3 µs.

Adr(@)	@+0	@+1	@+2	@+3	@+4	@+5	@+6	@+7	@+8	@+9	@+A	@+B	@+C	@+D	@+E	@+F
$0000	$80	$C0	$E0	$C0	$80	$40	$20	$40	$80	$C0	$E0	$C0	$80	$40	$20	$40
$0010	$80	$C0	$E0	$C0	$80	$40	$20	$40	$80	$C0	$E0	$C0	$80	$40	$20	$40
$0020	$80	$C0	$E0	$C0	$80	$40	$20	$40	$80	$C0	$E0	$C0	$80	$40	$20	$40
$0030	$80	$C0	$E0	$C0	$80	$40	$20	$40	$80	$C0	$E0	$C0	$80	$40	$20	$40

Tableau 2 : contenu partiel de la mémoire EPROM TEST

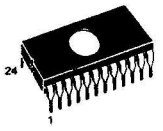
Le programme complet de l'EPROM est fourni sur disquette.

SGS-THOMSON MICROELECTRONICS

M2732A

NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS and OUTPUTS TTL COMPATIBLE DURING READ and PROGRAM
- COMPLETELY STATIC



FDIP24W (F)

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is honsed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the clerice by following the programming procedure.

Table 1. Signal Names

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

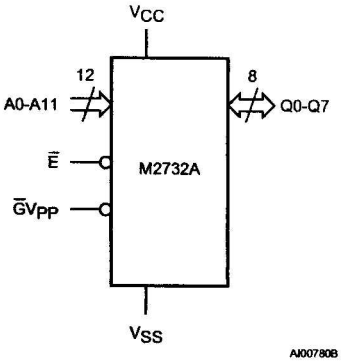
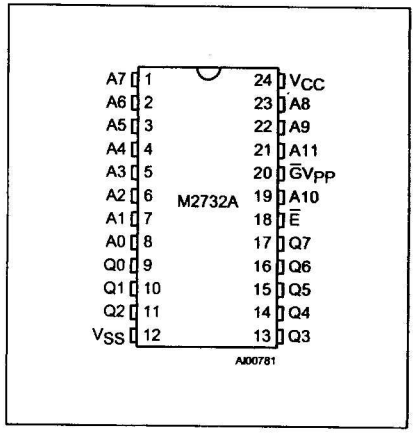


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6	V
V_{CC}	Supply Voltage		–0.6 to 6	V
V_{PP}	Program Supply Voltage		–0.6 to 22	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{E}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{E}$ be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.