

**REFERENCE**

du  
**COMPOSANT**



fabriquant  
du composant

3 PORTES NAND  
à 3 ENTREES

date de creation  
du document (octobre 1987)

October 1987

Revised August 2000

également mise  
à jour août 2000

**CD4023BC**

**Buffered Triple 3-Input NAND Gate**

TAMPON

**General Description**

DESCRIPTION

**Features**

CARACTERISTIQUES

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

- Wide supply voltage range: 3.0V to 15V
- High noise immunity:  $0.45 V_{DD}$  (typ)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage  $1 \mu A$  at 15V over full temperature range

TENSION  
d'ALIMENTATION  
de +3V à +15V

3 portes

**Ordering Code:**

NUMERO DU BOITIER UTILISE

Order Number	Package Number	Package Description
CD4023BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
CD4023BCS	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4023BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

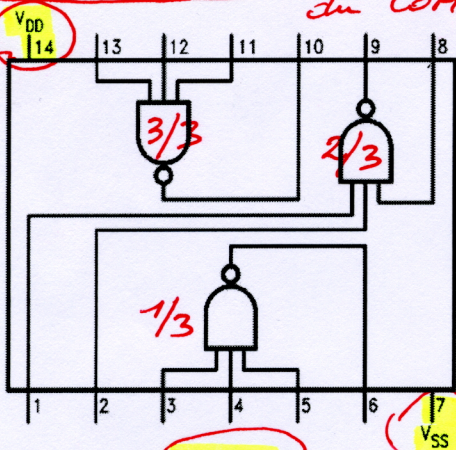
Description des  
BOITIERS

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

**Connection Diagram**

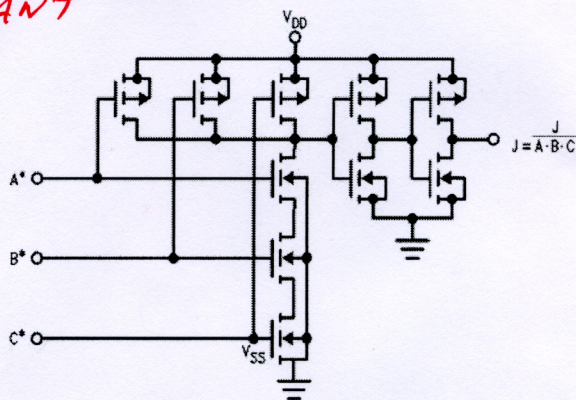
BROCHAGE Block Diagram  
du COMPOSANT

Alimentation  
(+3V à +15V)



Top View

Vue de dessus



1/3 Device Shown

\*All Inputs Protected by Standard CMOS Input Protection Circuit.

mette (0V)

A RETENIR : TRIPLE - INPUT - GATE - NAND - FEATURES

NUMBER - PACKAGE - TOP - VIEW - SUPPLY - RANGE

WIDE - CONNECTION DIAGRAM - DEVICE - BUFFER